IN THE SPECIFICATION:

Please delete the paragraph beginning on page 12, line 10, and replace with the following new paragraph. Changes from the original are highlighted.

Figure 23 shows a block diagram of an SMBus host controller 200. As explained above, the host controller comprises an ACPI-compliant register set 208. The memory address 209 of each register is specified by an offset of 0 to 40 to be added to a base address Base of the first register SMB_PRTCL. The host controller further comprises an address register array 207, a ROM 202 which stores several microcode sequences 210, 211 and 212, each comprising one or more instructions. The host controller comprises in addition a loop counter 204, an instruction fetch unit 203, including a program counter (designated "pc" in the box shown within instruction fetch unit 203), a finite-state machine 201, a buffer pointer 206, a PEC unit 215, and an SMBus interface comprising a clock line SMBCLK 213 and a data line SMBDAT 214.